MULTIFUNCTIONAL MEMORY CIRCUITS OF MARAKHOVSKY

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The article gives the limitations of the element base with memory on the flip-flops, the devices of which are described in automatic discrete time and the formulation is made to develop the extension of the properties of the element base due to memory on multifunctional circuits described in automatic continuous time. In the article a new definition of a multifunctional elementary automaton is given, a method of microstructural synthesis of such automata of two classes is considered, formulas are presented for establishing and preserving functions in automatic continuous time, and formulas are given that determine the basic parameters of elementary memory circuits. At the end of the article, examples of functional schemes of two classes of multifunctional memory circuits are given. In conclusion, the advantages of multifunction schemes over triggers are given.

Keywords: triggers, multifunctional memory circuits, automatic continuous time

Throughout the world, the search for new circuit-based solutions of elementary memory circuits with qualitatively new properties continues [1–5]. Unfortunately, all the works on the tunable memory scheme under consideration were carried out due to tunable excitation functions and outputs based on the RS trigger, which have fundamental limitations [6]:

1. They all work in the automaton discrete time t_i (i = 1, 2. …, n,…);
2. The basic memory scheme (*RS*-trigger) for known triggers does not allow you to rebuild the work of memorized states;
3. All these devices are described by the Mealy and Moore automata, which determine the sequential nature of the operation of the devices;
4. The transition in memory circuits occurs in one variable $x(t)$;
5. The principle of program management proposed by Charles Bebbage does not allow the simultaneous processing of general and local information and determines the division of information into only two parts.

In connection with these fundamental limitations of the class of monofunctional memory circuits (triggers), multifunctional memory schemes are proposed based on new principles and methods of structural organization.

The principle of the structured organization of multifunctional memory circuits (MFIS) is that n logical elements OR-NOT (AND-NOT) are used, which are divided into m ($m < n$) groups. The outputs of the elements of one group are not associated with the inputs of their group of logical elements. They are connected to the inputs of the elements of other groups of the memory scheme according to one of the defined laws (for example, with the inputs of all other logical elements or the inputs of only elements of two, three, etc. of m groups of elements). One of the free inputs of each i-th element is connected to the inputs of the setting input bus, and the second of the free inputs of each i-th element is connected to the inputs of the memory bus that stores the input bus. The introduction of an additional saving input bus in the memory scheme and the creation of groups of logical elements in a group of more than one was a fundamentally new phenomenon in the development of multifunctional memory circuits.

The principle of memorizing states in an MFIS is that the input signals that establish $x_i(t)$ that arrive at the nodes of the setting input bus uniquely determine the output active values of at least one logical element of the i-th group.

The output active values of the installed element through their output structural bonds keep the output values of other elements of the memory circuit inverted, which in turn through the inverse structural connections confirm the established output values of the logic elements when one of the conserved sets of input signals supplied by the conserving input bus. These set values of the state of the memory circuit $a(\Delta)$ are stored due to the state preservation functions δ_e until the next input $x_i(t)$ input signal arrives [7].

The use of state conservation functions δe in monofunctional Miley and Moore automata (also in memory circuits (triggers)) was not considered, because all triggers kept their states only with one passive input signal $e(\Delta)$, which was called an "empty word of zero length" although this function physically existed. In automatic discrete time, there was no length (interval Δ) for it, and under its influence no single transition from one state to another was realized. But this input signal $e(\Delta)$ has always been taken into account by the developers of memory circuits.

Definition 1. The MFIS will be called a single-level multifunctional elementary automaton (MEA) with a complete transition system and a complete output system for each of the r_e ($r_e > 1$) state conservation functions δ_e.

MEAs can be functionally represented as re single-level elementary automata, each of which remembers all its states only with one of the various corresponding sets of input signals that preserve $e_j(\Delta)$ ($j = \overline{1, r_e}$) [7].

Method of microstructural synthesis of elementary multifunctional memory circuits

Consider a method of microstructural synthesis, which allows us to construct an asynchronous MFIS class L from the logical elements of a functionally complete system.

We use the combination scheme OR-NOT, which realizes this function:

$$y = \overline{f(a) \vee f(x) \vee f(e)}, \qquad (1)$$

where $f(a)$ – is a function of an arbitrary input signal coming from the output of an element of another group for storing the state in the MFIS;
$f(x)$ – is a function of an arbitrary set of input signal $x_i(t)$;
$f(e)$ – is a function of an arbitrary saving $e_j(\Delta)$ set of the input signal.

The combination scheme (1) is called a basic automaton with one state or simpler than a basic automaton (BA). The simplest BA are logical elements of the AND-OR-NOT, OR-NOT or NAND type.

The method of microstructural synthesis of asynchronous MFIS of class L consists of the following algorithm. We take n BA and divide them into m ($m < n$) groups. The BA in each i-th group (i = 1, 2, ..., m) has no feedback, because their output nodes do not join the input nodes of the BA of this i-th group. The outputs of the BA of the i-th group are respectively connected directly or through the OR (AND) separation scheme or directly to the inputs $f(a)$ of all BAs of the other groups.

One of the free inputs z_i of each i-th BA is connected to the inputs of the setting input bus ШХ, and the second of the free inputs u_i of each i-th BA is connected to the inputs storing the input bus ШЕ of the memory circuit. Input nodes z_i can receive input $x_i(t)$ input signals, and input $e_i(\Delta)$ inputs can be input sequentially one by one for one clock cycle T_i ($T_i = t_i + \Delta_i$). Stable output signals at the output nodes yj of the BA correspond to the shifted states $a_j(T)$ of the MFIS, where $a_j(T) = a_i(t) + a_i(\Delta)$. The shift of the output signal $y_j(T)$ is equal to the delay of two logic elements, which is necessary to establish a stable output state in the memory circuit.

The $x(t)$ input signals of the MFIS unambiguously establish a certain state aj(t) of the memory circuit. The excitation function δ_x in an elementary automaton can be described in vector form:

$$a_i(t) = \delta_x[x(t)]. \qquad (2)$$

The value of the binary set at the input nodes z_j of the multifunctional memory scheme, under the action of the input signal setting $x(t)$, is characterized by the fact that only at the input nodes of the logical elements (BA_j) of one i-th group, the input signal can have a value equal to the passive signal 0 (1) On at least one logical element (BA_j) of this i-th group. At the input nodes of logic elements (BA_j) of other groups, the values of the input signal must be equal to the active signal 1 (0). The MFIS stored signal $e_j(\Delta)$ can memorize one of the states $a_j(\Delta)$ defined by the state block π_j, predetermined by the setting input signal x_i(t). The function δ_e of conservation of a state in an elementary automaton can be described in vector form:

$$a(T) = \delta_e[a(T), e(\Delta)],\ a(t) = a(\Delta). \qquad (3)$$

The value of the binary set at the input nodes uj of the MFIS under the action of the saving $e(\Delta)$ input signal is characterized by the fact that at least two MFIS groups at the input nodes of the BA have input signals whose value is equal to the passive signal 0 (1). The number K of storage states for a given $e(\Delta)$ input signal is equal to the number of groups in the MFIS, at the inputs of which the value of the input signal at node u_j is equal to the passive signal 0 (1). Thus, the value of the number K can vary depending on the input signals $e(\Delta)$ saving from 2 to m. The state a_i of the MFIS is identified with the state of the values of the output signals y_j BA_j of only one group if at least one of the output signals y_j of this group is equal to the active signal 1 (0). The unit value of the output signal y_j in this group is called the MFIS, because this output signal y_j acts on the BA_j of other groups, setting on them output signals y_j equal to the logical zero. The characteristic number K_i of the storage states of the i-th group is calculated by the formula:

$$K_i = 2^R - 1, \qquad (4)$$

where R is the BA number in the i-th group of the MFIS.

The number K_i of the storage states of the i-th group of the MFIS is a block of μ_i states. The transition from the state a_k to the state a_s in the block of μ_i states is possible with a change in the $e(\Delta)$ input signal. Such a transition is called enlarged. The function δ_y of the coarse transition can be represented in vector form:

$$a(\Delta) = \delta_y[a(t), e(\Delta)];$$
$$a(t) \neq a(\Delta); a(t), a(\Delta) \in \mu_i. \qquad (5)$$

Table 1

Setting the block *n* states of monofunctional memory circuits

e \ x_i	x_1	x_2	----	x_K
e_0	A_1	A_2	---	A_K

Table 2

Specifying the state matrix of multifunctional memory circuits

e_j \ x_i	x_1	x_2	---	x_K
e_1	A_{11}	A_{21}	---	A_{K1}
e_2	A_{12}	A_{22}	---	A_{K2}
---	---	---	---	---
e_m	A_{1m}	A_{2m}	---	A_{Km}

Thus, the number of memory states of an MFIS can be represented in a matrix form, where the rows of the matrix determine the blocks of π_i states that are remembered for the corresponding input signals retaining $e_j(\Delta)$, and the matrix columns are the states μ_i blocks that are set by the corresponding setting $x_i(t)$ input signals. A single-valued transition from the state a_i in the state a_k of the π_j state block (in the matrix row) is performed under the influence of the input signals establishing the $x_i(t)$ and the enlarged transition to the new state in the μi state block – under the influence of the preserving $e(\Delta)$ Input signals trigger circuits and SMEs have only one block of π states. This characteristic indicates that monofunctional memory circuits (triggers and SMEs) is a particular case of the MFIS. Consider tables of tasks for monofunctional (Table 1) and multifunctional (Table 2) memory schemes, which supports this conclusion.

The function φ of the outputs in the MFIS depends on the setting input word $p = x, e$, which establishes and stores the states a. In this case, two cases are possible: when the function δ_e of conservation of state (3) or the function δ_y of the coarse transition (5) is realized.

The function φ_1 of the outputs, which depends on the state of the automaton $a(\Delta - 1)$ and sets the input signal $x(t)$, characterizes the first-order automaton and in the vector form has the form:

$$y(t) = \varphi_1 [a(\Delta - 1), x(t)]. \quad (6)$$

The function φ_2 of the outputs depends on the state $a(t)$ of the state and on the stored $a(\Delta)$ state, which characterizes the automaton of the second kind and in the vector form has the form:

$$y(T) = \varphi_2 [a(t), a(\Delta)]; a(t) = a(\Delta), \quad (7)$$

or

$$y(T) = \varphi_2 [a(T)], a(T) = a(t) \cup a(\Delta). \quad (8)$$

The function φ_2 outputs ensures that the set state $a(T)$ is maintained for a continuous cycle time T.

The function φ_3 of the outputs in the MFIS depends on the set a(t) state and on the stored input signal $e(\Delta)$ and which can be represented in vector form as follows:

$$y(\Delta) = \varphi_3 [a(t), e(\Delta)]. \quad (9)$$

The function φ_3 outputs characterizes automata of the third kind, which determines the direction of the output signal $y(\Delta)$ as a function of the saving signal $e(\Delta)$.

Description of elementary multifunctional memory circuits

The most famous binary elementary memory circuits are triggers based on the *RS*-trigger [4-6], which is a particular case of the MFIS [2]. Such schemes are characterized by three main parameters: M – the number of stable states a, each of which corresponds to a certain output signal of the memory circuit $y_2(T)$; r_x – is the number of setting input signals $x(t)$ and r_e – is the number of conserved input signals $e(\Delta)$,

which are formally associated with the MFIS structure. The basic MFIS structures created on NAND or NOR logical elements are called basic automata (BA), and their parameters are determined by the proposed formulas.

Memory circuits consist of groups BA (elements), the groups of which are interconnected by feedback circuits, and the characteristic number of memory states K_i in the i-th group is determined by the formula (4). Thus, the number M of stable states $a(\Delta)$ of the MFIS stored under the influence of the input signals retaining $e(\Delta)$ is determined by the formula:

$$M = \sum_{i=1}^{m} K_i, \qquad (4.10)$$

where K_i – is the characteristic number of states in the ith group of the MFIS.

The total number r_x of different sets of $x(t)$ input signals set by the MFIS is given by:

$$r_x = M + 1, \qquad (11)$$

where M – is the number of stable states of the MFIS, which are conserved;
1 – is an additional set of the input signal that sets $x_p(t)$, which uniquely establishes the state $a_r(t)$, which is not conserved for any set of the MFIS stored $e(\Delta)$ input signal. Such a set of $x_p(t)$ input signal in deterministic devices is forbidden [5].

The total number r_e of different sets of e (Δ) inputs that are stored in the MFIS can be defined by the formula

$$r_e = \prod_{i=1}^{m} K_i. \qquad (12)$$

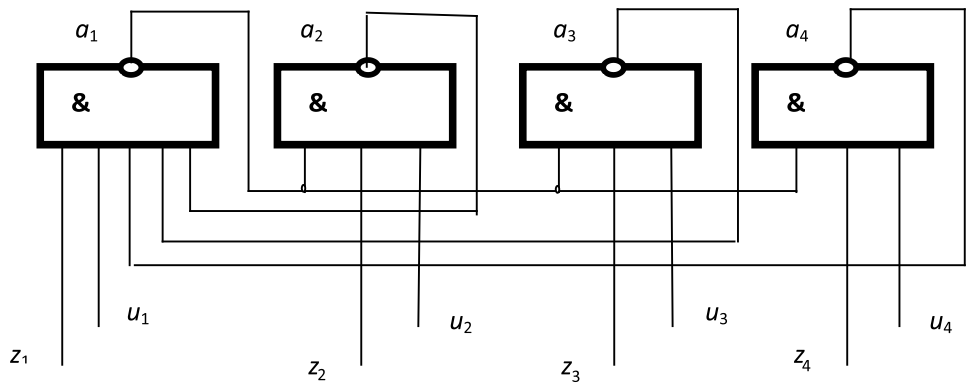

Fig. 1. MFIS class L on the elements of the AND-NOT

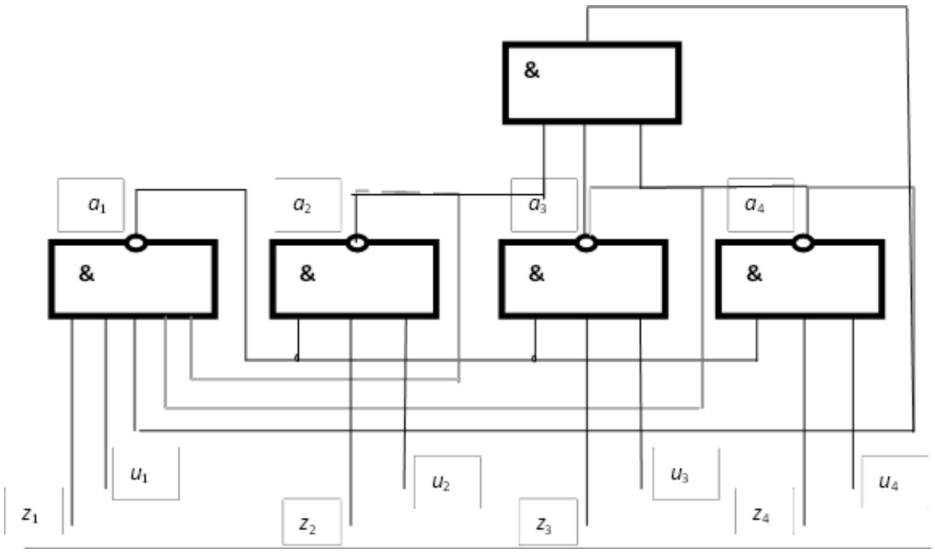

Fig. 2. MFIS class LM on the elements of the AND-NOT

Thus, it becomes clear that two sets of input signals are required for the operation of multifunctional circuits: setting and saving $e_j(\Delta)$, which enter one clock cycle of T ($T = t + \Delta$). A feature of these two sets of input signals is that the setting xi (t) absorbs the preserving $e_j(\Delta)$ if they arrive at the same hour.

$$x_i(t) = x_i(t) \bigcup e_j(t) . \qquad (13)$$

Logical elements of one group are connected by their output nodes to the input nodes of all logical elements of other groups. Other inputs of logic elements (at least two) that connect to the corresponding input MFIS buses are used for setting and storing input signals. The output nodes of the logic elements are connected to the output line of the MFIS.

Let us consider an example of the synthesis of the functional scheme of an MPSE on the elements AND-NOT of two classes L and L^M.

An important functional advantage of MFIS over flip-flops and SMBs is the possibility of reconstructing the structure of the memory states during operation for one machine clock T, otherwise it can be said that an increase in the degree of freedom from 1 to re is determined.

Conclusion

Multifunctional memory circuits have the advantage over the basic binary memory scheme of the *RS*-flip-flop. MISPs reduce the hardware costs per stored state; increase the functionality by realigning the structure of state storage and simultaneously processing the levels of hierarchical information represented as sets of input-preserving signals $e(\Delta)$ as general and local information represented as sets of input signals $x(t)$ in one machine clock cycle T.

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