

OPTIMIZATION OF SEMIBRIDGE TRANSISTOR INVERTERS CONTROL SYSTEMS

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The article deals with a half-bridge inverter operation system which allows automatically coordinate the duration of enabling pulses at the control input of transistors with the necessary duration of their switching-on, thus reducing breaks in transistors.

Keywords: transistor, voltage sensor, logical gate, capacity

Transistor inverters, both single-cycle and duple, have found a wide application as components of various secondary power supplies [1, 2].

A special version of duple inverters is a semibrige inverter.

In the semibrige inverter the necessary duration of the stage «or» decreases with the growth of loading, i.e. the necessary duration of the stage «on» can be much less than the duration of unlocking impulses produced by control system output and it leads to unjustified losses in transistors.

To decrease these losses two logic double input elements «&» and two voltage gauges at semibrige transistor inverter capacitors are included into the semibrige transistor inverter control system, the voltage gauges outputs and the semibrige transistor inverter control system outputs being connected to the double input logic elements «&» inputs, the outputs of double input logic elements «&» being connected to the corresponding control transistors inputs of a semibrige transistor inverter. It has allowed to coordinate the duration of unlocking impulses at the control transistor inputs of a semibrige transistor inverter automatically with the desired duration of the stage «on» and, thus, to reduce the losses.

The control system (Fig. 1) functions as follows. When voltage U is applied, capacitors 4 and 5 are charged up to 0,5 V. Let's apply a voltage impulse from control system 2 to logic element «&» input 13. The other input of element 13 has also got a signal from voltage gauge 11, and a logic unit will be sent to transistor input 6 from logic double input element «&» 13 and transistor 6 will be «on».

If the loading current is small, capacitor 4 during an unlocking impulse will not have time to get discharged and transistor 6 will be unlocked during this time.

When the unlocking impulse from control system 2 disappears the impulse from the second output of control system 2 does not act. This pause is necessary for locking properties of a transistor to be restored, the duration of a pause being stipulated in a typical control

system 2. After a pause the unlocking impulse from control system 2 comes to the input of logic double input element «&» 14. There is a signal from voltage gauge 12 at the second input of element «&» 14 and an unlocking impulse comes to transistor input 7. Then the cycle repeats.

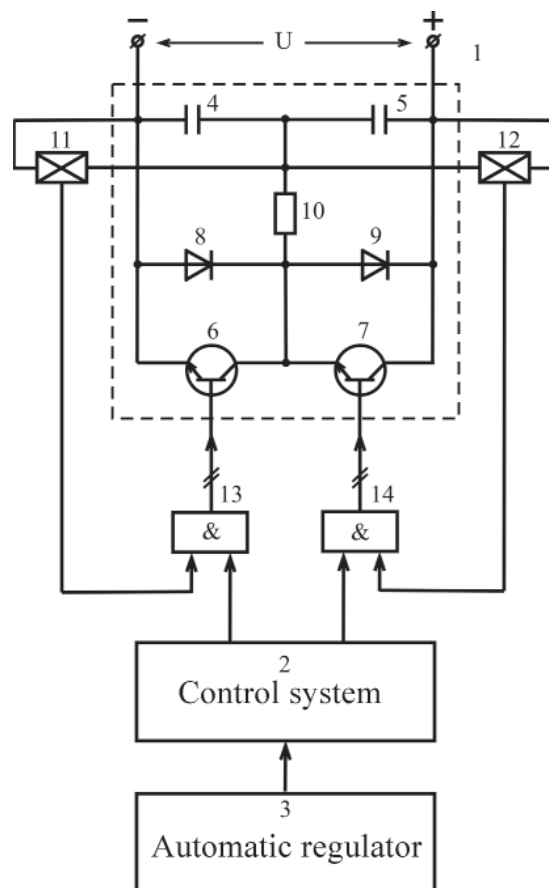


Fig. 1. The inverter control systems

Thus, at small loading current the duration of unlocked state of transistors 6, 7 is determined only by the «width» of an unlocking impulse from control system 2.

If the loading current exceeds some critical value I_{cr} (Fig. 2), capacitors 4 and 5 will have time to discharge completely during a half-

cycle of an inverter operation. In this mode the control system provides constant loading capacity ($U_d I_d = \text{const}$). As soon as the voltage at capacitor 4, for instance, reaches zero, the «unit» at the logic element output 13 will disappear, transistor 6 will be locked and the electromagnetic energy accumulated in loading 10 will be discharged in the circuit: loading 10 – diode 9 – capacitors 5 – loading-10. Besides, the discharge current will flow through output capacity of a power supply.

The losses in transistor 6 are excluded in this interval and the electromagnetic energy accumulated in loading partially comes to capacitor 5 and pack to the power supply. It is obvious that the greater the loading current, the higher the efficiency of the scheme suggested.

For instance, of the inverter is used for supply via a stepping down transformer of an electric arc in a welding device, the control system functions either in an idle mode or at

current $> I_{cr}$. In this mode this control system sufficiently reduces unproductive losses in inverter transistors.

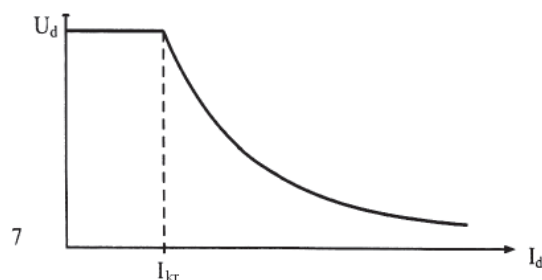


Fig. 2. The volt-ampere load characteristic

References

1. Transpoket // Austria, the catalogue. – 1995-1996.
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